1. Description

- The M7125 is a limiting low noise amplifier (LNA) fabricate on GaAs p-HEMT MMIC, integrated Limiter and LNA. It operates over 8-12GHz and achieves 1.1dB noise figure with 29dB gain.

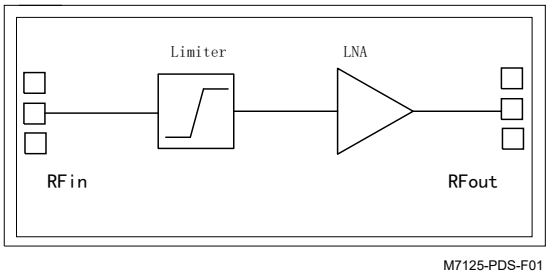


Figure 1. M7125 Functional Block Diagram

2. Applications

- TX/RX Modules
- Commercial and Military Radar
- Defense

3. Features

- Frequency Range: 8-12GHz
- Typical Gain: 29dB
- Noise Figure: 1.1dB
- Input/Output Return Loss: -15dB
- Output P_{-1dB}: 12dBm
- Saturated Output Power (P_{SAT}): 14dBm
- Power Handling Capability: 43dBm
- Single Positive Supply: +4V (I_{DQ}=65mA)
- Dimensions: 2.5 x 1.25 x 0.1 mm

4. Brief Typical Performance

Table 1. Brief Typical Performance

Parameter	8-12GHz	Units
Small-Signal Gain	29	dB
Noise Figure	1.1	dB
Input/Output Return Loss	-15	dB
Output P_{-1dB}	12	dBm
Output P_{SAT}	14	dBm
Power Handling Capability	43	dBm

Test Conditions: Input signal is pulsed, with a pulse width of 50μs and a duty cycle of 15%.

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5. Recommended Operating Conditions

Table 2. Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Units
Operating Temperature Range	-55	25	125	°C
Supply Voltage, V_D	-	4	-	V
Quiescent Current, I_{DQ}	-	65	-	mA

6. RF Characteristics （TC = 25°C）

Table 3. RF Characteristics[1]

Parameter	Symbol	Min.	Typ.	Max.	Units
Small-Signal Gain	Gain	-	29	-	dB
Gain Flatness	ΔG	-	±1	-	dB
Noise Figure	NF	-	1.1	-	dB
Input Return Loss	RL_{IN}	-	-15	-10	dB
Output Return Loss	RL_{OUT}	-	-15	-10	dB
Output Power for 1dB Compression	OP_{-1dB}	-	12	-	dBm
Saturated Output Power	P_{SAT}	-	14	-	dBm
Power Handling Capability	$P_{IN\ MAX}$	-	43	-	dBm

[1].Test Conditions: Input signal is pulsed, with a pulse width of 50μs and a duty cycle of 15%.

7. Typical Performance Curve (T_C = 25°C)

■ Small-signal Characteristics Curve (VD=4V, On-Wafer Test)

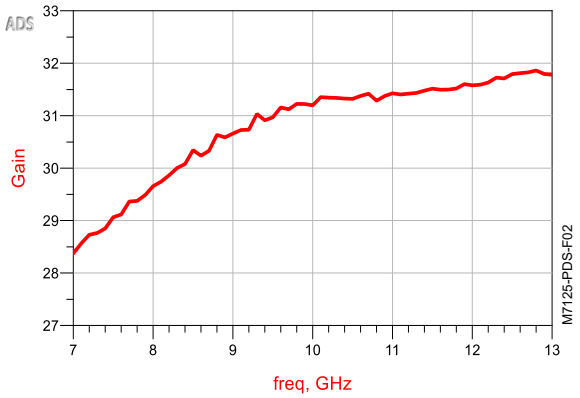


Figure 2. Small-signal Gain Characteristics

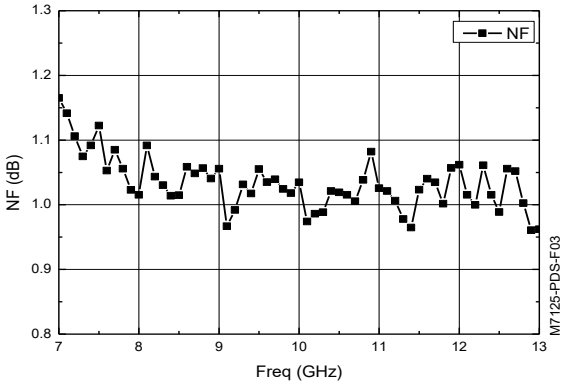


Figure 3. Noise Figure Characteristics

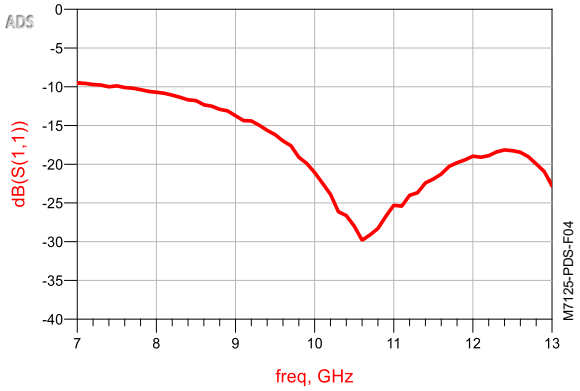


Figure 4. Input Return Loss Characteristics

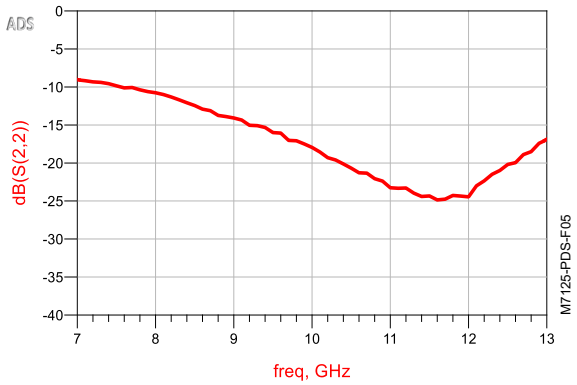


Figure 5. Output Return Loss Characteristics

■ Power Characteristic Curve (VD=4V, On-Wafer Test)

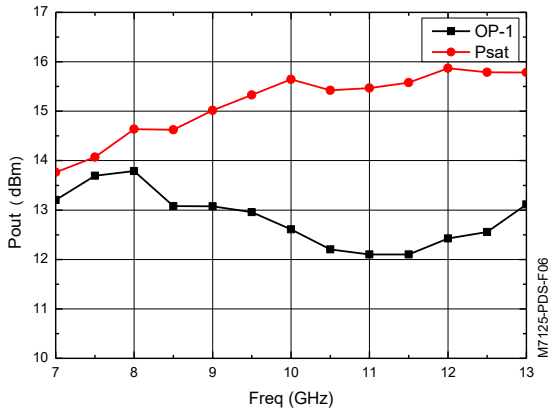
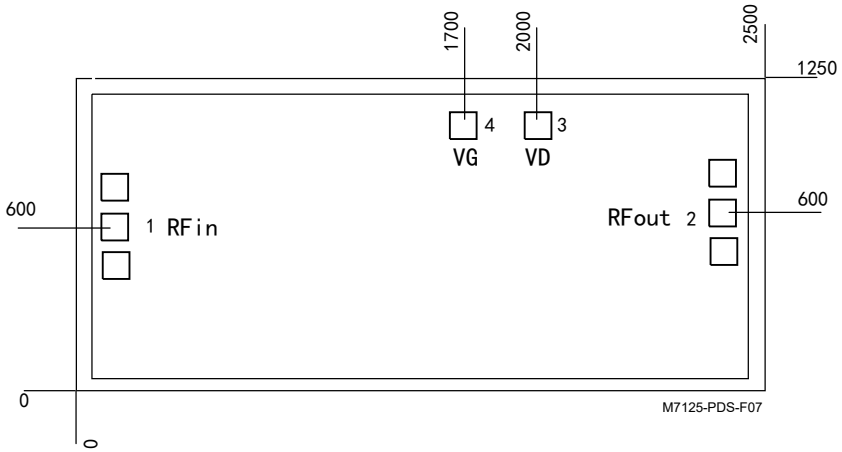


Figure 6. OP_{-1dB} / P_{SAT} Characteristics

8. Outline Dimensions



- Dimensions shown in micrometre

Figure 7. M7125 Outline Dimensions

Table 4. Pad Description

Pad	Symbol	Description
1	RF_{in}	RF Input
2	RF_{out}	RF Output
3	VD	Supply Voltage
4	VG	Supply Voltage

9. Assembly Information

■ Assembly Diagram

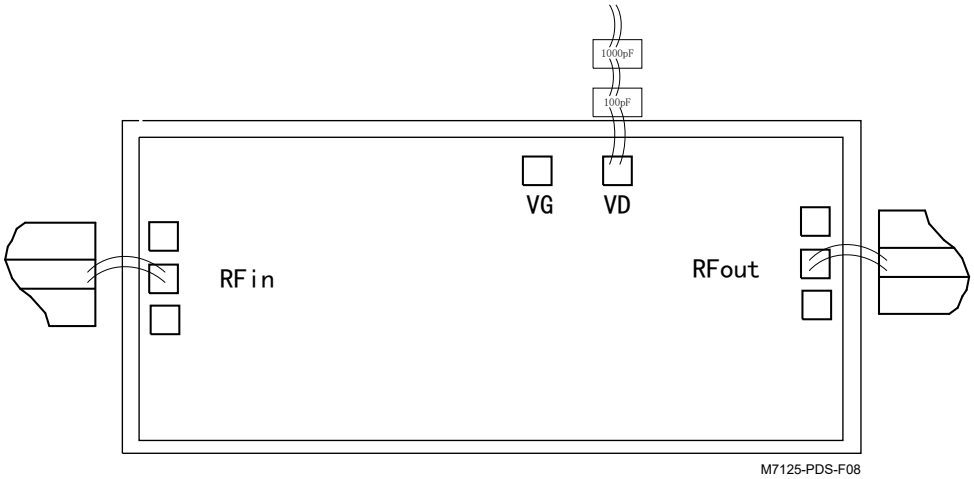


Figure 8. M7125 Assembly Diagram

- **Eutectic Die Attach:** It is best to use an 80% Au/20% Sn preform. Do not expose the chip to a temperature greater than 300°C for more than 30sec.
- **Wire Bonding:** RF bonds made with 1mil gold wire are recommended for the RF ports. Keep all bonds as short as possible, less than 0.35mm.

10. Handling Precautions

■ Storage

All bare dies ship in either Waffle or Gel Pak, which is an ESD protective container, and then sealed in an ESD protective bag. After opening the sealed ESD protective bag, all dies must be stored in a dry nitrogen environment.

■ Cleanliness

Handle the dies in a clean environment. Never use liquid cleaning systems to clean the dies.

■ ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore proper ESD precautions should be taken to avoid performance degradation or loss of functionality.



11. Contact Information

For the latest specifications, additional product information, technical support and sales support, please contact:

- **Email:** RF.support@raytrontek.com
- **Web:** www.raytrontek.com

12. Disclaimer

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