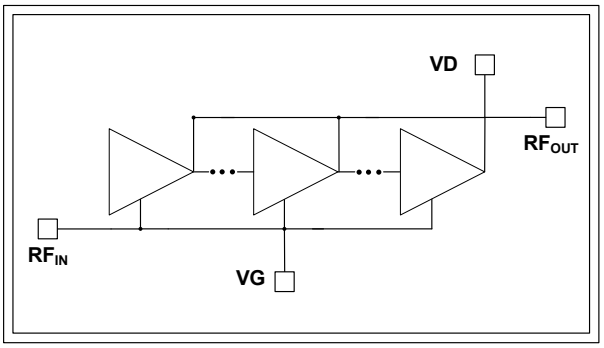
1. Description

- The M1767 is an 0.01-10GHz power amplifier manufactured using a 0.25μm gate-length gallium arsenide high electron mobility transistor (HEMT) process. The M1767 is grounded through backside metal via holes. All chips undergo 100% RF measurement.



M1767-PDS-F01

Figure 1. M1767 Functional Block Diagram

2. Applications

- TX/RX Modules
- Wireless Communications

3. Features

- Frequency Range: 0.01-10GHz
- Output Power (P_{SAT}): 28dBm (0.6W)
- Power Gain: 12dB
- Operating Bias: 8V (V_D), I_{DQ}=0.38A
- Small Signal Gain: 12dB
- Input Return Loss: -10dB
- Die Size: 3.50 x 2.80 x 0.10mm

4. Brief Typical Performance

Table 1. Brief Typical Performance

Parameter	0.01-10GHz	Units
Output Power	28	dBm
Power Gain	12.5	dB
Power Added Efficiency	12	%
Drain Dynamic Current	0.42	A
Small Signal Gain	13	dB
Input Return Loss	-10	dB
Output Return Loss	-10	dB

- Test condition: CW (continuous wave)

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5. Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Drain-Source Voltage	V_{DS}	9	V
Gate-Source Voltage	V_{GS}	-2	V
Maximum Input Power	P_{IN}	25	dBm
Maximum Forward Gate Current	$I_{G\ Max}$	10	mA
Storage Temperature Range	T_{STG}	-65 ~ +150	°C

6. Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Units
Operating Temperature Range	-55	25	85	°C
Drain-Source Voltage Range, V_{DS}	-	8	-	V
Drain Bias Current, I_{DQ}	-	0.38	-	A
Gate-Source Voltage, V_{GS}	-	-0.71	-	V

7. RF Characteristics (T_C = 25˚C)

Table 4. RF Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units
Output Power	P_{SAT}	27	28	28.5	dBm
Power Gain	G_P	11	12	12.5	dB
Power Added Efficiency	PAE	10	12	14	%
Drain Dynamic Current	Id	-	0.42	-	A
Small Signal Gain	Glin	12	13	22	dB
Input Return Loss	S11	-	-10	-	dB
Output Return Loss	S22	-	-10	-	dB

• Test condition: CW (continuous wave)

8. Typical Performance Curve

■ Small signal Characteristics Curve (T_C = 25˚C)

(V_D=8V, V_{G1}=-0.71V, V_{G2}=3V, I_{DQ}=0.38A, P_{IN}=-20dBm)

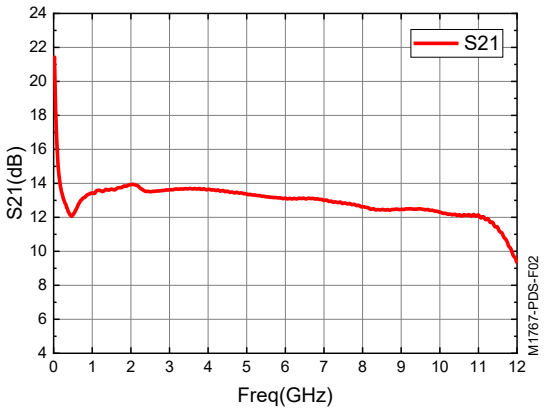


Figure 2. Small Signal Gain vs. Frequency

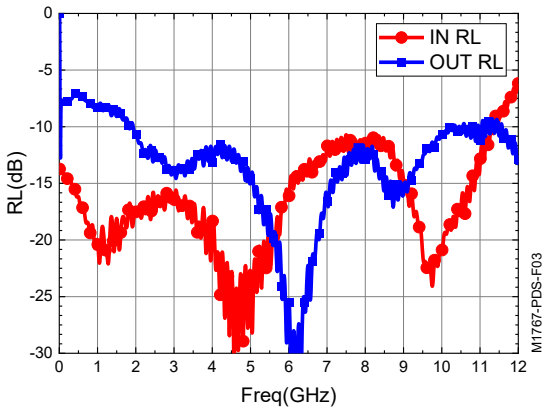


Figure 3. Input Return Loss vs. Frequency

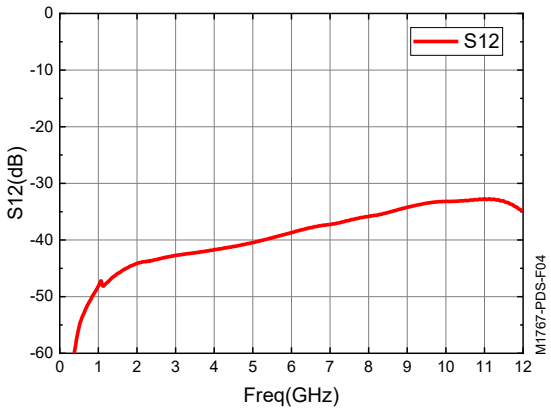


Figure4. Small Signal Isolation vs. Frequency

■ Power Characteristic Curve

（V_D=8V, V_{G1}=-0.71V, V_{G2}=3V, I_{DQ}=0.38A, P_{IN}=16dBm）

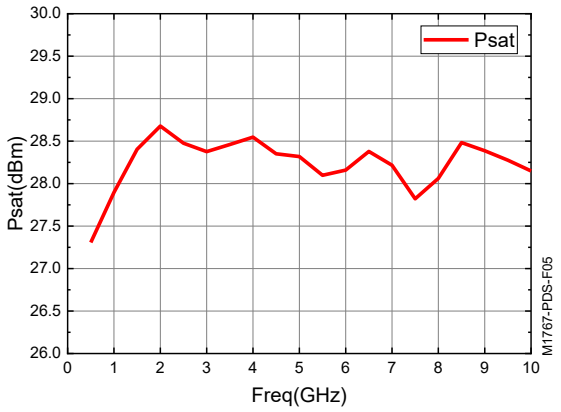


Figure 5. Output Power vs. Frequency

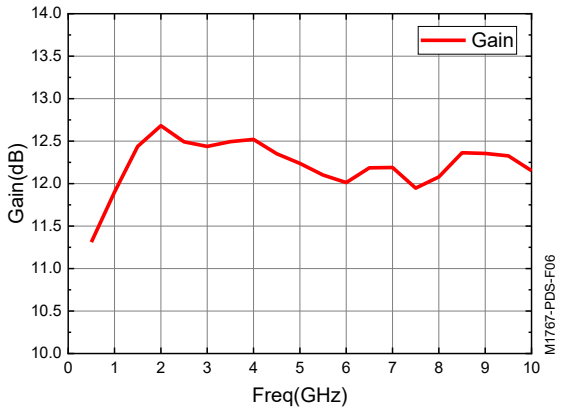


Figure 6. Power Gain vs. Frequency

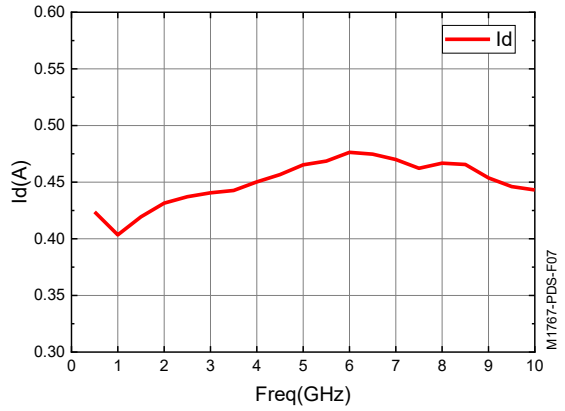


Figure 7. Drain Dynamic Current vs. Frequency

（V_D=12V，V_{G1}=-0.71V， V_{G2}=5V， I_{DQ}=0.38A，P_{IN}=20dBm）

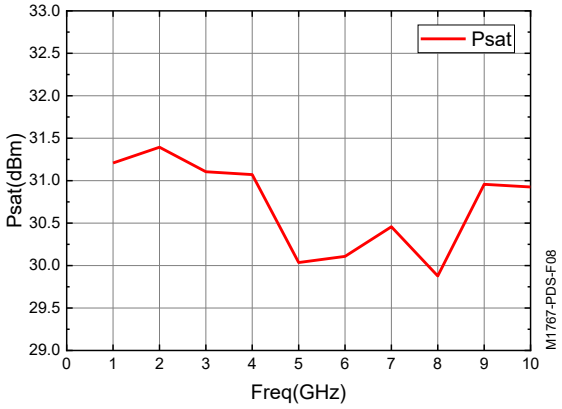


Figure 8. Output Power vs. Frequency

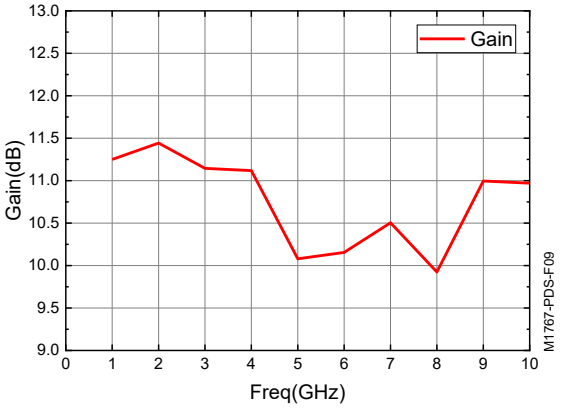


Figure 9. Power Gain vs. Frequency

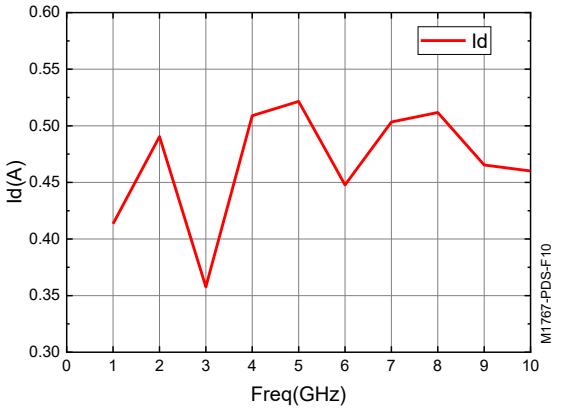


Figure 10. Drain Dynamic Current vs. Frequency

■ Output Third Order Intercept Point Characteristic Curve (T_C = 25˚C)

(V_D=8V, V_{G1}=-0.71V, V_{G2}=3V, I_{DQ}=0.38A, P_{OUT}=14dBm/tone)

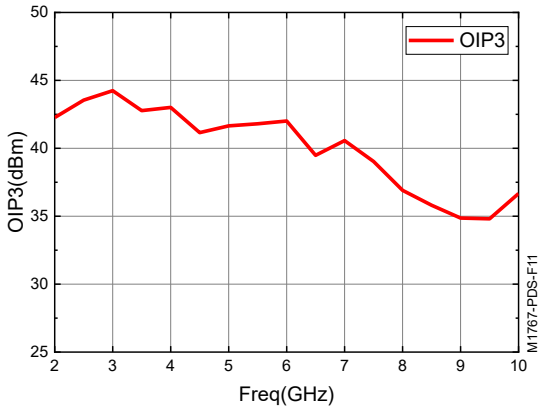


Figure 11. OIP3 vs. Frequency

(V_D=12V, V_{G1}=-0.71V, V_{G2}=5V, I_{DQ}=0.38A, P_{OUT}=20dBm/tone)

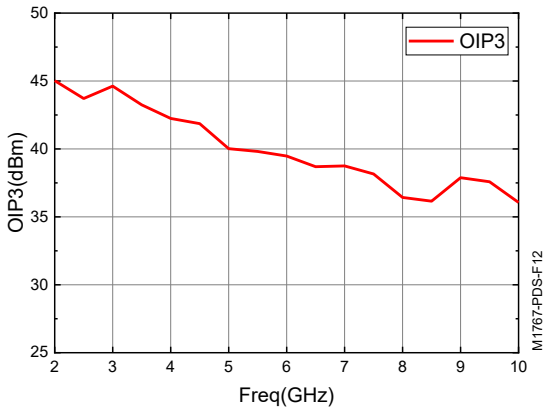
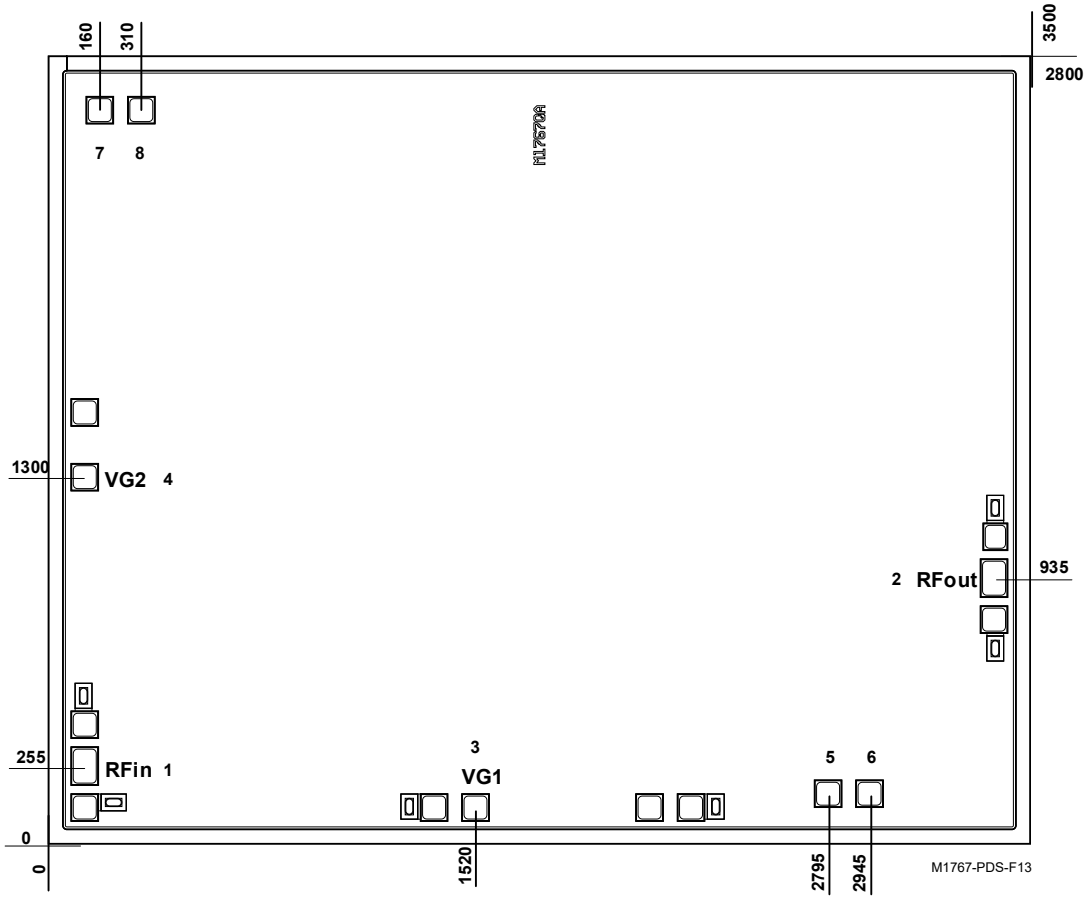


Figure 12. OIP3 vs. Frequency

9. Outline Dimensions



• Dimensions shown in micrometre

Figure 13. M1767 Outline Dimensions

Table 5. Pad Description

Pad	Symbol	Description
1	RF_{IN}	RF Input. 50Ω. DC blocking capacitor is required.
2	RF_{OUT}	RF Output. 50Ω. DC blocking capacitor is required.
3	V_{G1}	Gate Voltage. Bypass network required, refer to Figure 14.
4	V_{G2}	Gate Voltage. Bypass network required, refer to Figure 14.
5,6,7,8	RF_{GND}	Bypass network required, refer to Figure 14.

10. Assembly Information

■ Assembly Diagram

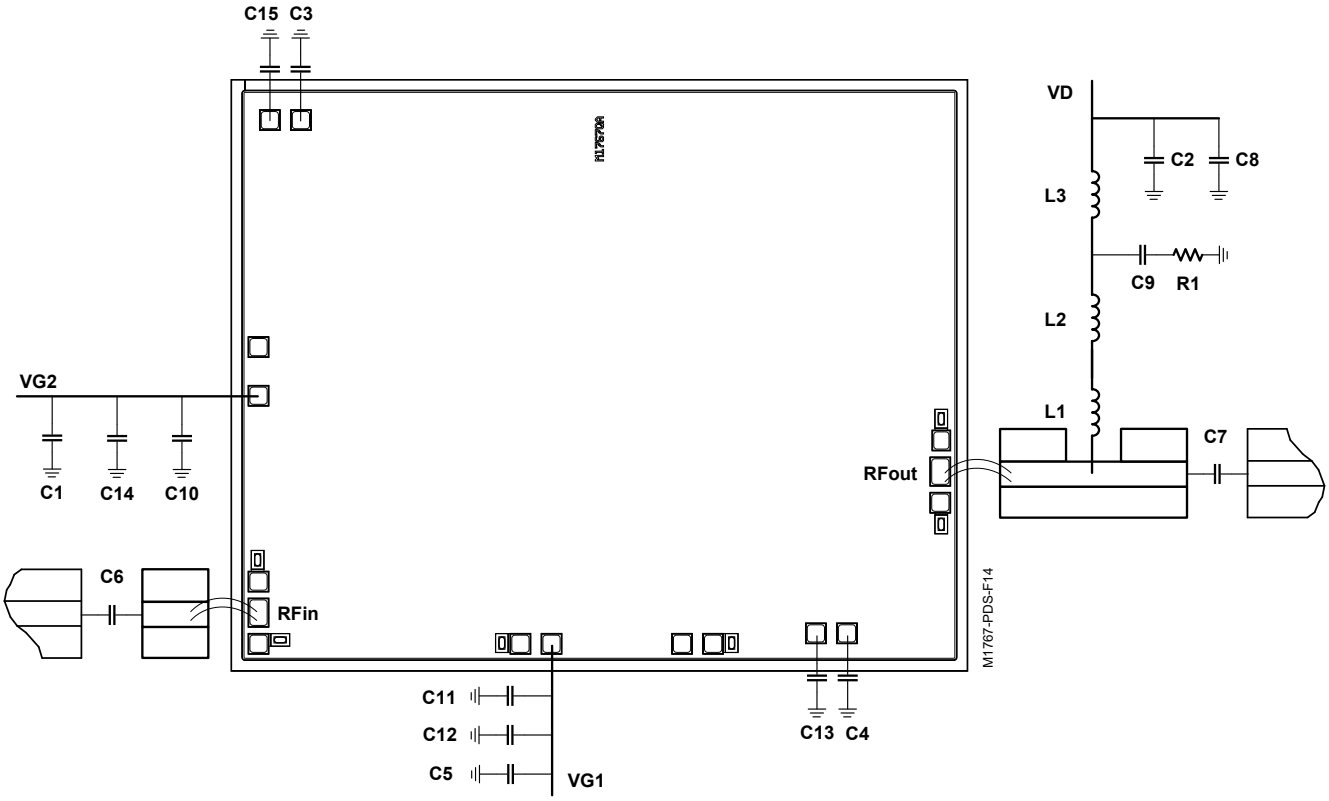


Figure 14. M1767 Assembly Diagram

Table 6. Component Description

Component	Value	Size
R1	301Ω	0402
C1,C2,C3,C4,C5	4.7uF	1206
C6,C7,C8	0.1uF	0402
C9,C10,C11	100uF	0402
C12,C13,C14,C15	1nF	0402
L1,L2	36nH	0402
L3	0.9uH	1008

- **Eutectic Die Attach:** It is best to use an 80% Au/20% Sn preform. Do not expose the chip to a temperature greater than 300°C for more than 30sec.
- **Wire Bonding:** RF bonds made with 1mil gold wire are recommended for the RF ports.

11. Handling Precautions

- **Storage**
  All bare dies ship in either Waffle or Gel Pak, which is an ESD protective container, and then sealed in an ESD protective bag. After opening the sealed ESD protective bag, all dies must be stored in a dry nitrogen environment.
- **Cleanliness**
  Handle the dies in a clean environment. Never use liquid cleaning systems to clean the dies.
- **ESD Caution**
  ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore proper ESD precautions should be taken to avoid performance degradation or loss of functionality.



12. Contact Information

For the latest specifications, additional product information, technical support and sales support, please contact:

- **Email:** RF.support@raytrontek.com
- **Web:** www.raytrontek.com

13. Disclaimer

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