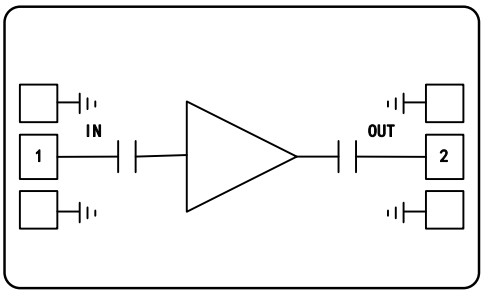
1. Description

- The M1766 is a 2-10GHz Ultra-wideband Distributed amplifier manufactured using a 0.25μm gate-length gallium arsenide high electron mobility transistor (pHEMT) process. The M1766 is grounded through backside metal via holes. All chips undergo 100% RF measurement.



M1766-PDS-F01

Figure 1. M1766 Functional Block Diagram

2. Applications

- TX/RX Modules
- Wireless Communications

3. Features

- Frequency Range: 2-10GHz
- Typical Gain: 11dB
- Noise Figure: <6dB
- Input/Output Return Loss: -12dB
- Output P Sat: 25dBm
- Single Positive Supply: +8V (I_{DQ}=180mA)
- Die Size: 2.70 x 1.45 x 0.10mm

4. Brief Typical Performance

Table 1. Brief Typical Performance

Parameter	2-10GHz	Units
Small-Signal Gain	11	dB
Noise Figure	6	dB
Input Return Loss	-12	dB
Output Return Loss	-20	dB
Output P_{SAT}	25	dBm

Test Conditions: Input signal is pulsed, with a pulse width of 100 μs and a duty cycle of 10%.

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5. Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Drain-Source Voltage	V_{DS}	10	V
Maximum Input Power	P_{IN}	20	dBm
Storage Temperature Range	T_{STG}	- 65 ~ +150	°C

6. Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Units
Operating Temperature Range	-55	25	125	°C
Drain-Source Voltage Range, V_{DS}	-	8	-	V
Drain Bias Current, I_{DQ}	-	180	-	mA

7. RF Characteristics (T_C = 25°C)

Table 4. RF Characteristics[1]

Parameter	Symbol	Min.	Typ.	Max.	Units
Small-Signal Gain	Gain	-	11	-	dB
Noise Figure	NF	-	6	-	dB
Input Return Loss	RL_{IN}	-	-12	-	dB
Output Return Loss	RL_{OUT}	-	-20	-	dB
Saturated Output Power	P-sat	-	25	-	dBm

[1] Test Conditions: Input signal is pulsed, with a pulse width of 100 μs and a duty cycle of 10%.

8. Typical Performance Curve (T_C = 25°C)

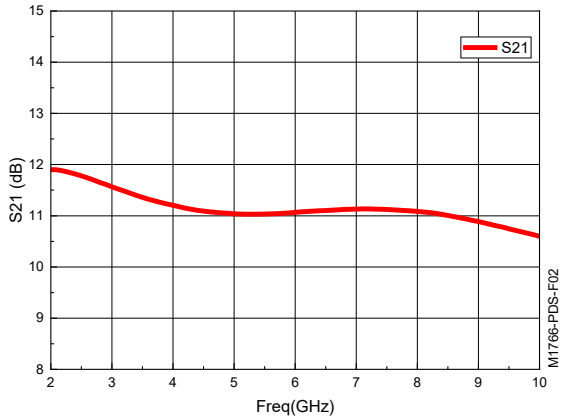


Figure 2. Small Signal Gain vs. Frequency

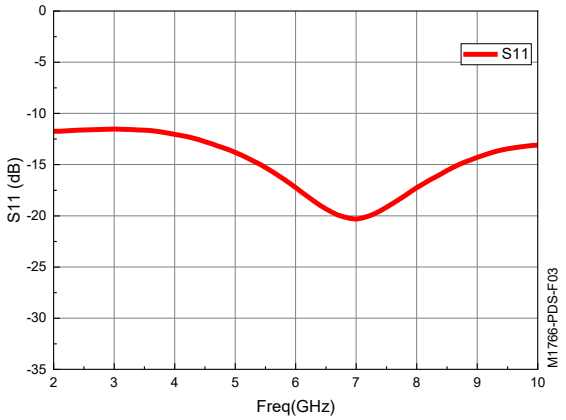


Figure 3. Input Return Loss vs. Frequency

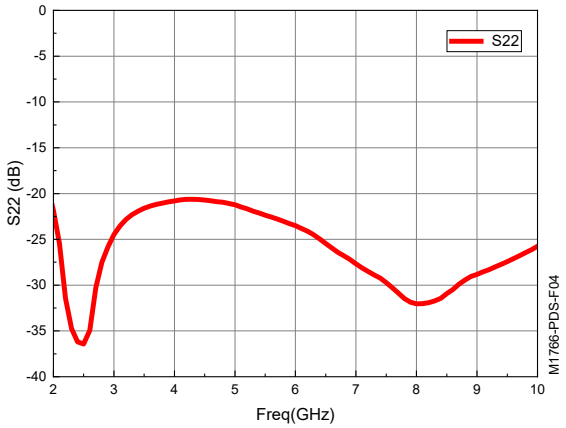


Figure 4. Output Return Loss vs. Frequency

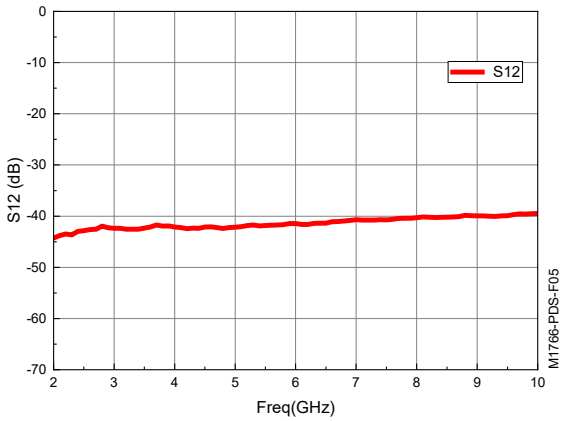


Figure 5. Reverse Isolation vs. Frequency

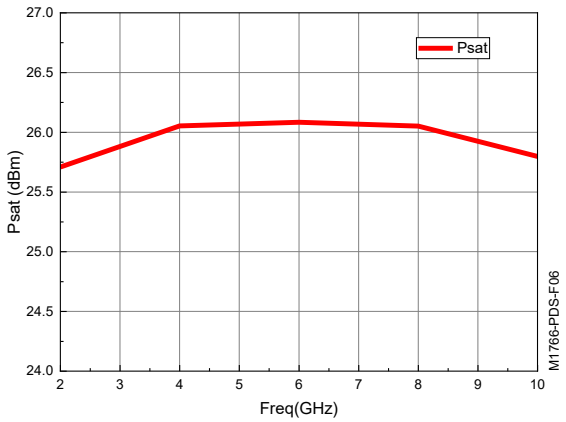


Figure 6. P-Sat Characteristics

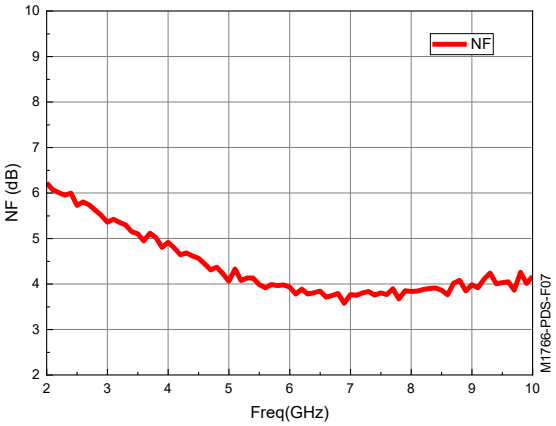
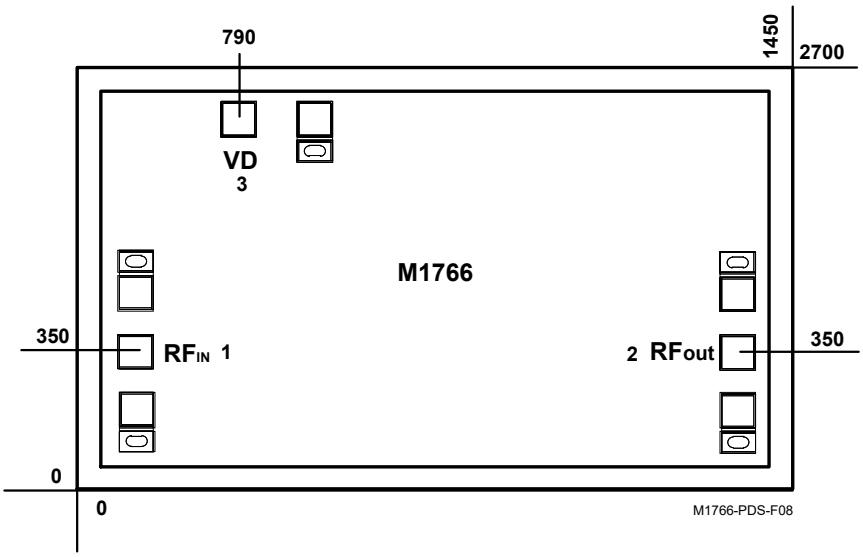


Figure 7. Noise Figure Characteristics

9. Outline Dimensions



• Dimensions shown in micrometre

Figure 8. M1766 Outline Dimensions

Table 5. Pad Description

Pad	Symbol	Description
1	RFin	RF Input. 50Ω. DC blocking capacitor is not required.
2	RFout	RF Output. 50Ω. DC blocking capacitor is not required.
3	VD	Supply Voltage. External bypass capacitors are required, refer to Figure 9.

10. Assembly Information

■ Assembly Diagram

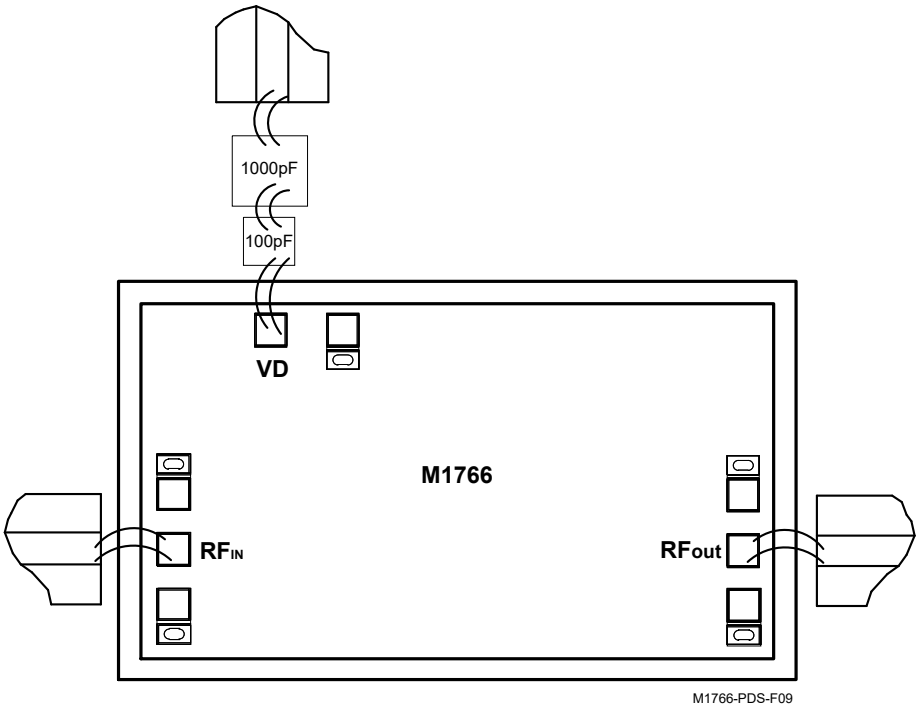


Figure 9. M1766 Assembly Diagram

- **Eutectic Die Attach:** It is best to use an 80% Au/20% Sn preform. Do not expose the chip to a temperature greater than 300°C for more than 30sec.
- **Wire Bonding:** RF bonds made with 1mil gold wire are recommended for the RF ports.

11. Handling Precautions

■ Storage

All bare dies ship in either Waffle or Gel Pak, which is an ESD protective container, and then sealed in an ESD protective bag. After opening the sealed ESD protective bag, all dies must be stored in a dry nitrogen environment.

■ Cleanliness

Handle the dies in a clean environment. Never use liquid cleaning systems to clean the dies.

■ ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore proper ESD precautions should be taken to avoid performance degradation or loss of functionality.



12. Contact Information

For the latest specifications, additional product information, technical support and sales support, please contact:

- **Email:** RF.support@raytrontek.com
- **Web:** www.raytrontek.com

13. Disclaimer

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