1. Description

- The M1717E is an 8-12GHz power amplifier integrated power detector manufactured using a 0.25μm gate-length gallium arsenide high electron mobility transistor (HEMT) process. The M1717E is grounded through backside metal via holes. All chips undergo 100% RF measurement.

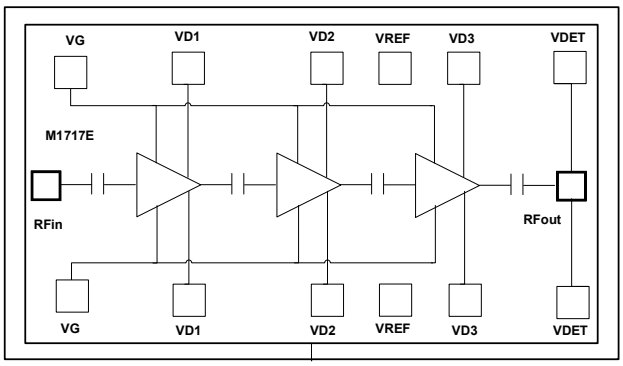


Figure 1. M1717E Functional Block Diagram

2. Applications

- TX/RX Modules
- Wireless Communications

3. Features

- Operating Frequencies: 8-12GHz
- Output Power (P_{SAT}): 34.8dBm (3W)
- Power Gain: 28dB
- Typical Power Added Efficiency: 35%
- Operating Bias: 8V (V_D), I_{DQ}=0.8A
- Small Signal Gain: 30dB
- Input Return Loss: -9dB
- Power Detected Voltage: 3V
- Die Size: 3.10 x 1.80 x 0.08mm

4. Brief Typical Performance

Table 1. Brief Typical Performance

Parameter	8-12GHz	Units
Output Power	34	dBm
Power Gain	28	dB
Power Added Efficiency	35	%
Drain Dynamic Current	1.5	A
Small Signal Gain	30	dB
Input Return Loss	-9	dB
Output Return Loss	-15	dB

- Test condition: Input signal and V_D Pulsed, Small Signal test Pulse width=100ms, Power test Pulse width=10μs, Duty cycle=10%

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5. Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Drain-Source Voltage	V_{DSS}	9	V
Gate-Source Voltage	V_{GS}	-2	V
Operating Voltage Range	V_{DS}	0 ~ +8	V
Maximum Input Power	P_{IN}	25	dBm
Maximum Forward Gate Current	$I_{G\ Max}$	10	mA
Storage Temperature Range	T_{STG}	- 65 ~ +150	°C
Operating Junction Temperature	T_J	175	°C

6. Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Units
Operating Temperature Range	-55	25	85	°C
Drain-Source Voltage Range, V_{DSS}	-	8	-	V
Drain Bias Current, I_{DQ}	-	0.85	-	A
Gate-Source Voltage, V_{GS}	-	-0.65	-	V

7. RF Characteristics (T_C = 25˚C)

Table 4. RF Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units
Output Power	P_{SAT}	34	34.8	36	dBm
Power Gain	G_P	28	29	30	dB
Power Added Efficiency	PAE	30	35	45	%
Drain Dynamic Current	I_D	0.9	1.2	1.5	A
Small Signal Gain	G_{SS}	28	31	33	dB
Input Return Loss	S11	-	-9	-	dB
Output Return Loss	S22	-	-15	-	dB
Power Detected Voltage	V_{DELTA}	2	3	4	V

• Test condition: Input signal and V_D Pulsed, Small Signal Test Pulse width=100ms, Power Test Pulse width=10μs, Duty cycle=10%

8. Typical Performance Curve

■ Small signal Characteristics Curve (TC = 25˚C)

(V_D=8V，V_G=-0.65V，I_{DQ}=0.8A，P_{IN}=-20dBm，Pulse width=100us，Duty cycle=10%)

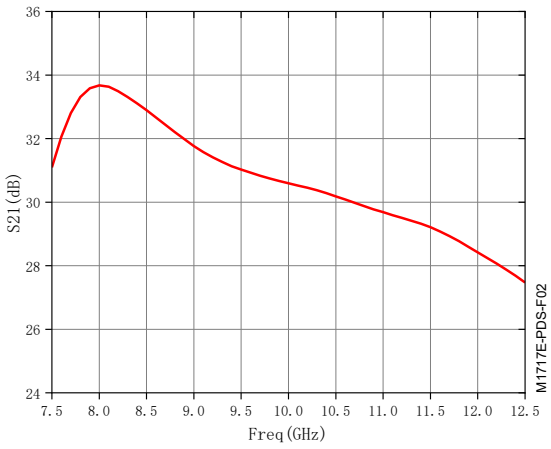


Figure 2. Small Signal Gain vs. Frequency

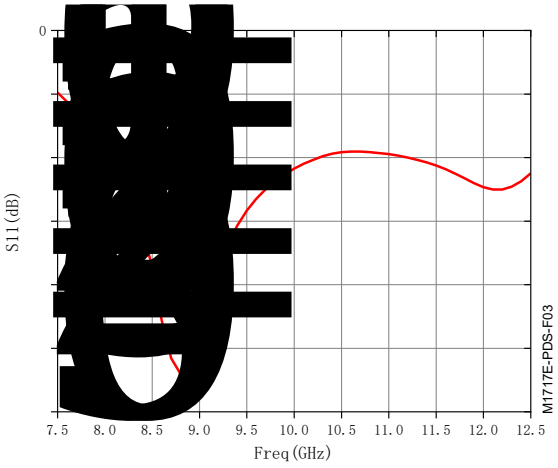


Figure 3. Input Return Loss vs. Frequency

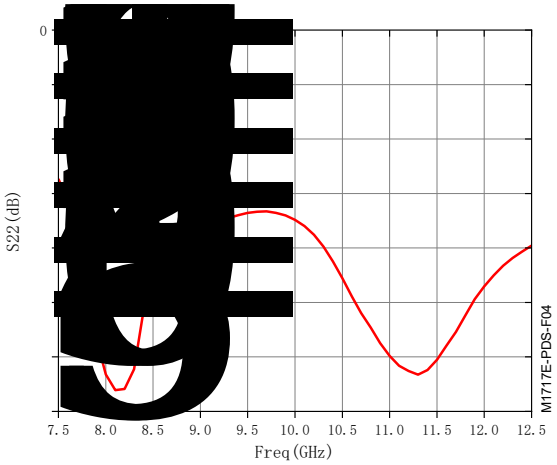


Figure 4. Output Return Loss vs. Frequency

■ Power Characteristic Curve

（ V_D=8V，V_G=-0.65V，I_{DQ}=0.8A，P_{IN}=6dBm，Pulse width=10μs，Duty cycle=10%）

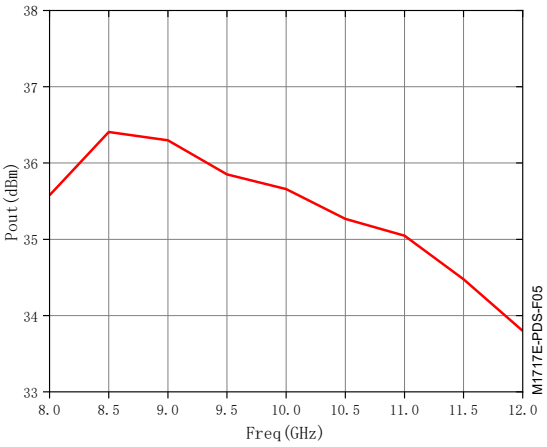


Figure 5. Output Power vs. Frequency

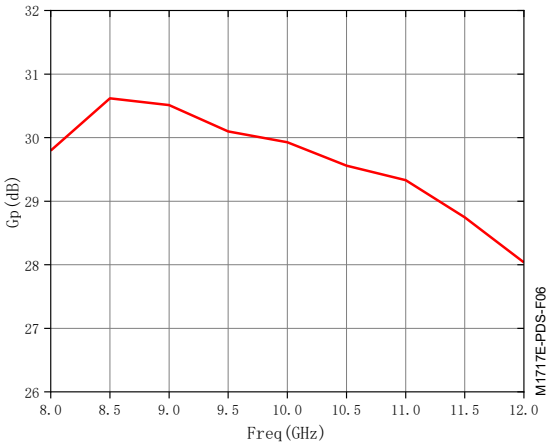


Figure 6. Power Gain vs. Frequency

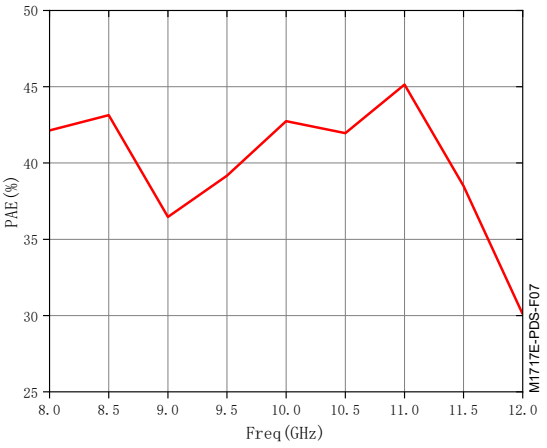


Figure 7. Power Added Efficiency vs. Frequency

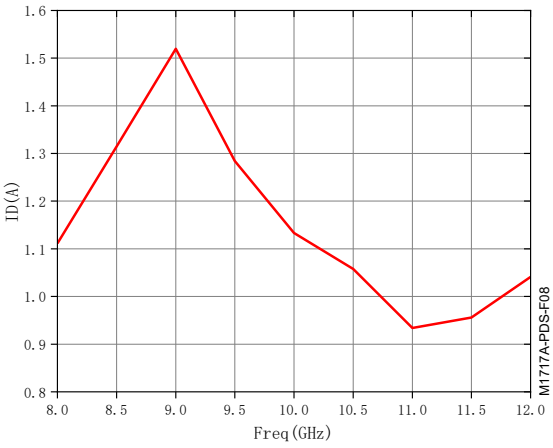


Figure 8. Drain Dynamic Current vs. Frequency

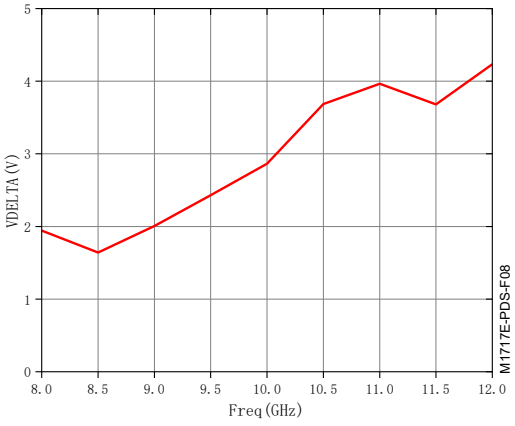


Figure 8. Detector Voltage at Psat vs. Frequency (V_{DELTA}=V_{REF}-V_{DET})

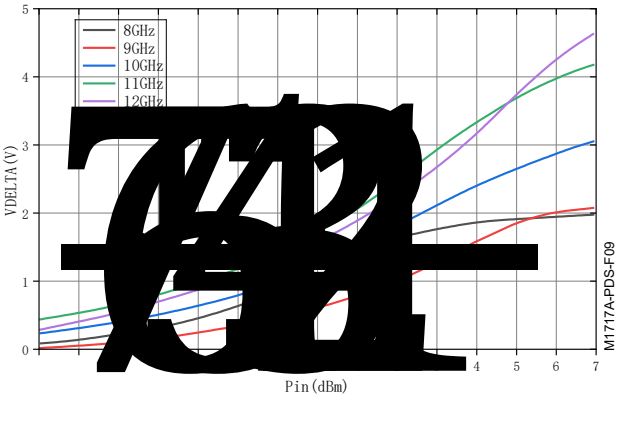
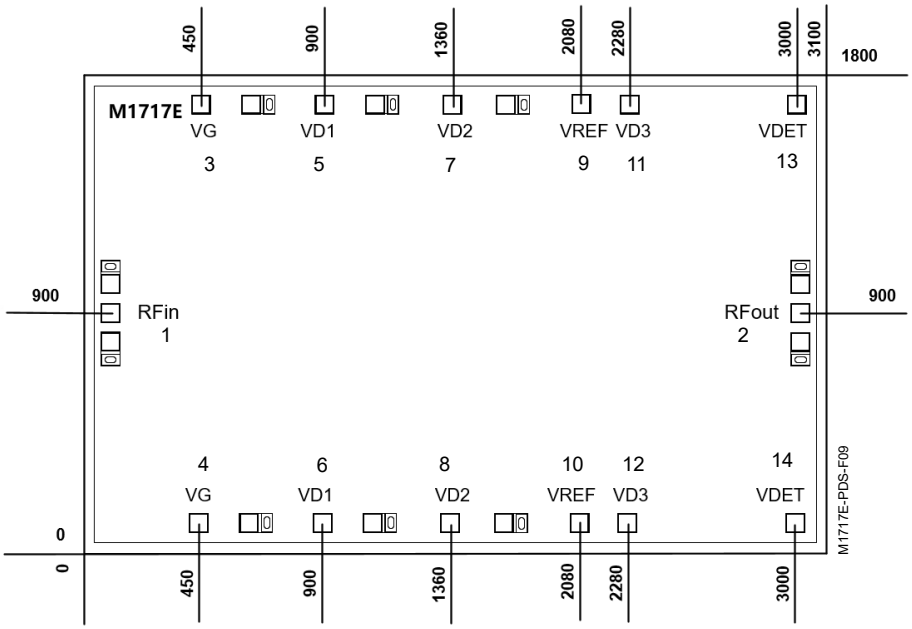


Figure 9. Detector Voltage vs. Frequency vs. Pin

9. Outline Dimensions



• Dimensions shown in micrometre

Figure 9. M1717E Outline Dimensions

Table 5. Pad Description

Pad	Symbol	Description
1	RF_{IN}	RF Input. 50Ohms. DC blocking capacitor is not required.
2	RF_{OUT}	RF Output. 50Ohms. DC blocking capacitor is not required.
3,4	V_G	Gate Voltage stage1&2&3. Bypass network required, refer to figure 10.
5,6	V_{D1}	Drain Voltage stage1. Bypass network required, refer to figure 10.
7,8	V_{D2}	Drain Voltage stage2. Bypass network required, refer to figure 10.
9,10	VREF	Reference voltage for Power detector
11,12	V_{D3}	Drain Voltage stage3. Bypass network required, refer to figure 10.
13,14	VDET	Power detector voltage.

10. Assembly Information

■ Assembly Diagram

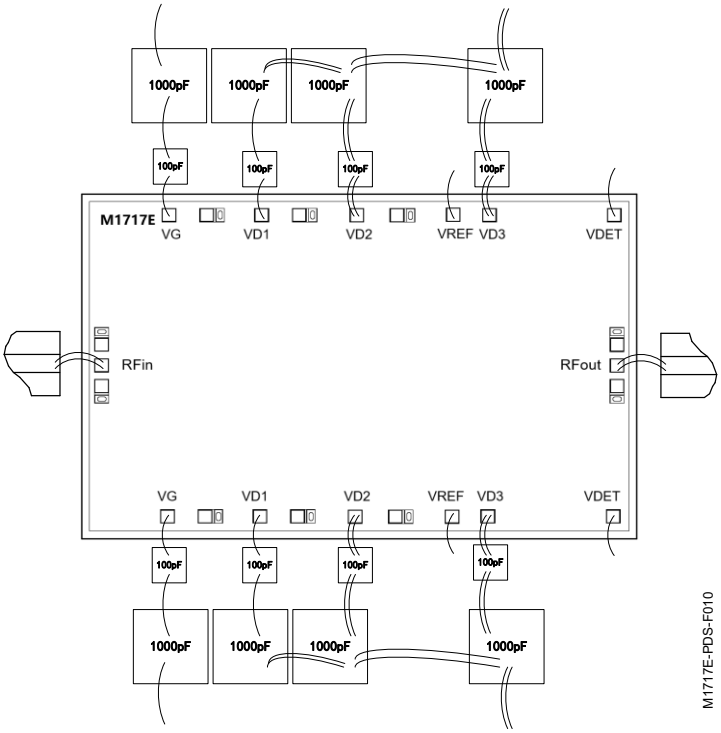


Figure 10. M1717E Assembly Diagram

- **Eutectic Die Attach:** It is best to use an 80% Au/20% Sn preform. Do not expose the chip to a temperature greater than 300°C for more than 30sec.
- **Wire Bonding:** RF bonds made with 1mil gold wire are recommended for the RF ports.

11. Handling Precautions

■ Storage

All bare dies ship in either Waffle or Gel Pak, which is an ESD protective container, and then sealed in an ESD protective bag. After opening the sealed ESD protective bag, all dies must be stored in a dry nitrogen environment.

■ Cleanliness

Handle the dies in a clean environment. Never use liquid cleaning systems to clean the dies.

■ ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore proper ESD precautions should be taken to avoid performance degradation or loss of functionality.



12. Contact Information

For the latest specifications, additional product information, technical support and sales support, please contact:

- **Email:** RF.support@raytrontek.com
- **Web:** www.raytrontek.com

13. Disclaimer

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