1. Description

- The M1711Q is an 11-16 GHz power amplifier fabricated in a 0.25-μm GaAs pHEMT process. It is available in a low-cost, surface-mount 16 leads,3mmx3mm QFN package and is ideally suited for Point-to-Point Radio and Ku-Band VSAT ground terminals. All devices are 100% RF tested.



M1711Q-PDS-F01

Figure 1. M1711Q Package Outline

2. Applications

- Point-to-Point Radio
- Ku-band VSAT
- Ku-band Phase Array

3. Features

- Operating Frequencies: 11-16GHz
- P_{1dB}: 26dBm
- P_{SAT}: 26.5dBm
- Power Gain: 21dB
- Operating Bias: 5V (V_D), I_{DQ}=300mA
- Small Signal Gain: 24dB
- OTOI:32 dBm at 16dBm/tune
- Input Return Loss: -13dB
- Output Return Loss: -10dB
- Package: 3.00 x 3.00 x 0.85mm QFN

4. Brief Typical Performance

Table 1. Brief Typical Performance

Parameter	Typical Value	Units
Operational Frequency Range	11-16	GHz
Small Signal Gain	24	dB
Power Gain	21	dB
Output Power at 1dB Compression	26	dBm
Output Power at Saturation	26.5	%
Drain Dynamic Current	400	mA
Input Return Loss	-13	dB
Output Return Loss	-10	dB

- Test condition: V_D=5V，V_G=-0.55V，I_{DQ}=300mA，CW，25°C. Data de-embedded to device reference plane.

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5. Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Drain-Source Voltage	V_{DS}	6	V
Gate-Source Voltage	V_{GS}	-2	V
Maximum Input Power	P_{IN}	15	dBm
Maximum Forward Gate Current	$I_{G\ Max}$	10	mA
Storage Temperature Range	T_{STG}	-65 ~ +150	°C

6. Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Units
Operating Temperature Range	-40	25	85	°C
Drain Voltage, V_{DS}	-	5	-	V
Drain Bias Current, I_{DQ}	-	300	-	mA
Gate Voltage(typical), V_{GS}	-	-0.55	-	V

7. RF Characteristics (T_C = 25˚C)

Table 4. RF Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating Frequencies	Freq.	11	-	16	GHz
Small Signal Gain	G_{SS}	22	24	24	dB
Power Gain	G_P	19.5	21	21.6	dB
Output Power at 1dB Compression	P_{1dB}	25.2	26	27.3	dBm
Output Power at Saturation	P_{SAT}	25.5	26.5	27.9	dBm
Output TOI (@ Drain Current of 320mA)	OTOI	-	32	-	dBm
Drain Dynamic Current	I_D	-	400	-	mA
Input Return Loss	S11	-	-13	-	dB
Output Return Loss	S22	-	-10	-	dB

• Test condition: V_D=5V，V_G=-0.55V，I_{DQ}=300mA，CW，25°C. Data de-embedded to device reference plane.

8. Typical Performance Curve

■ Small signal Characteristics Curve (T_C = 25˚C)

(V_D=5V, V_G=-0.55V, I_{DQ}=300mA, CW)

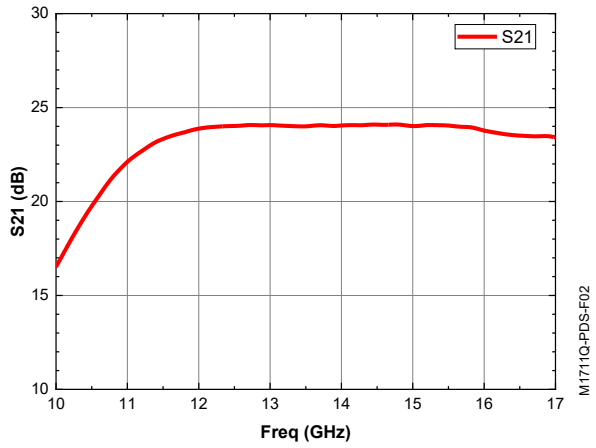


Figure 2. Small Signal Gain vs. Frequency

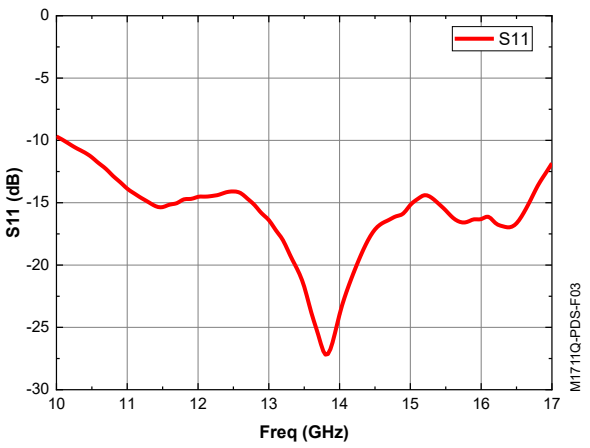


Figure 3. Input Return Loss vs. Frequency

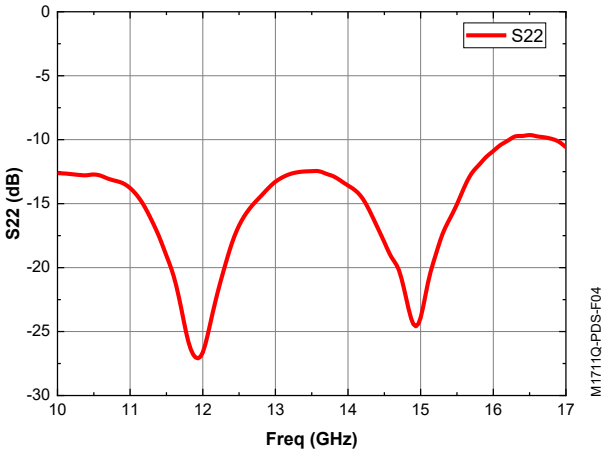


Figure 4. Output Return Loss vs. Frequency

■ Power Characteristic Curve

（V_D=5V，V_G=-0.55V，I_{DQ}=300mA，CW）

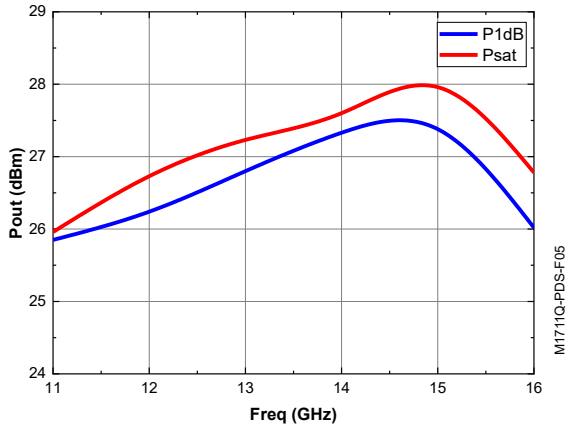


Figure 5. Output Power vs. Frequency

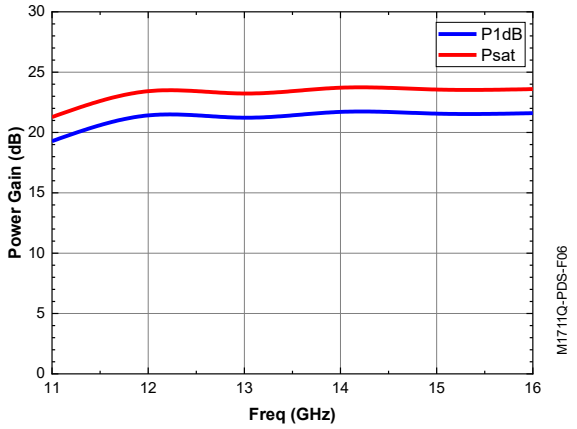


Figure 6. Power Gain vs. Frequency

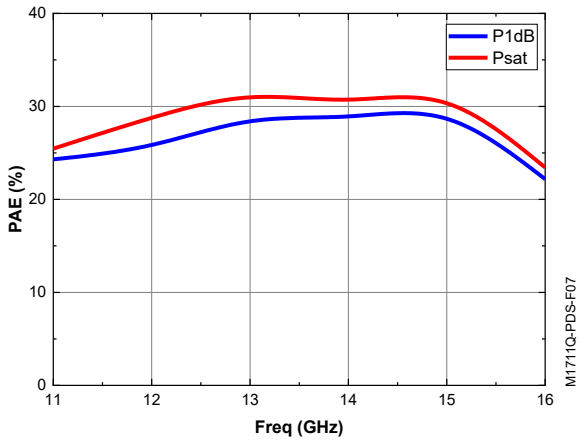


Figure 7. Power Added Efficiency vs. Frequency

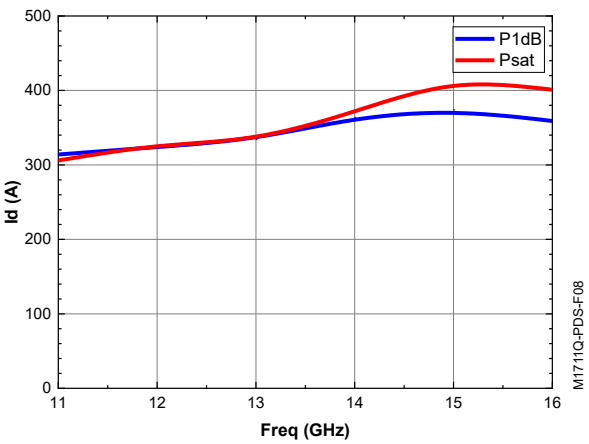


Figure 8. Drain Dynamic Current vs. Frequency

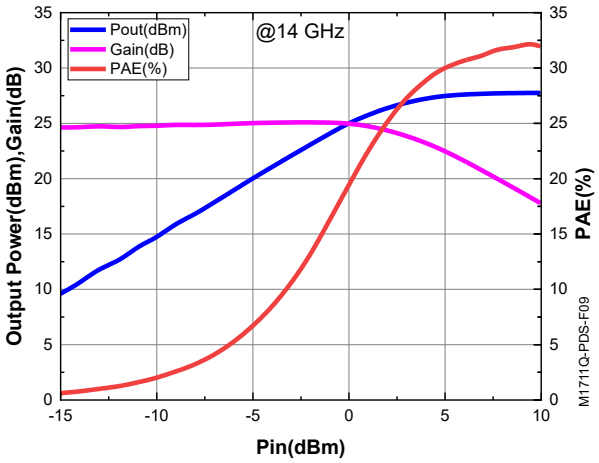


Figure 9. Output Power, Gain, PAE vs. Input Power

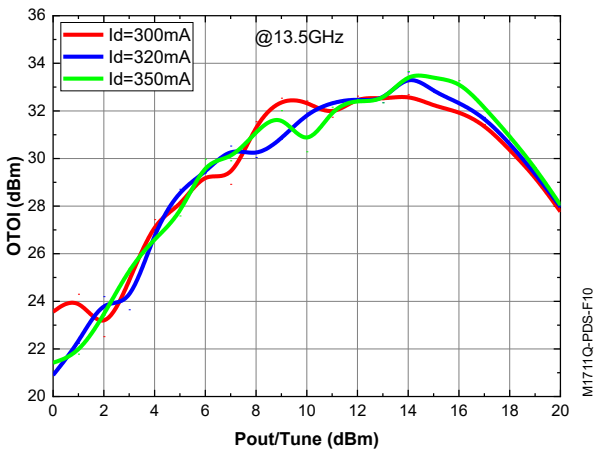


Figure 10. Output TOI vs. Pout/Tune

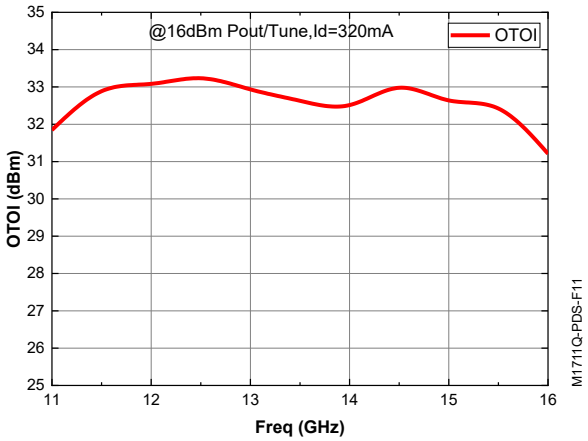
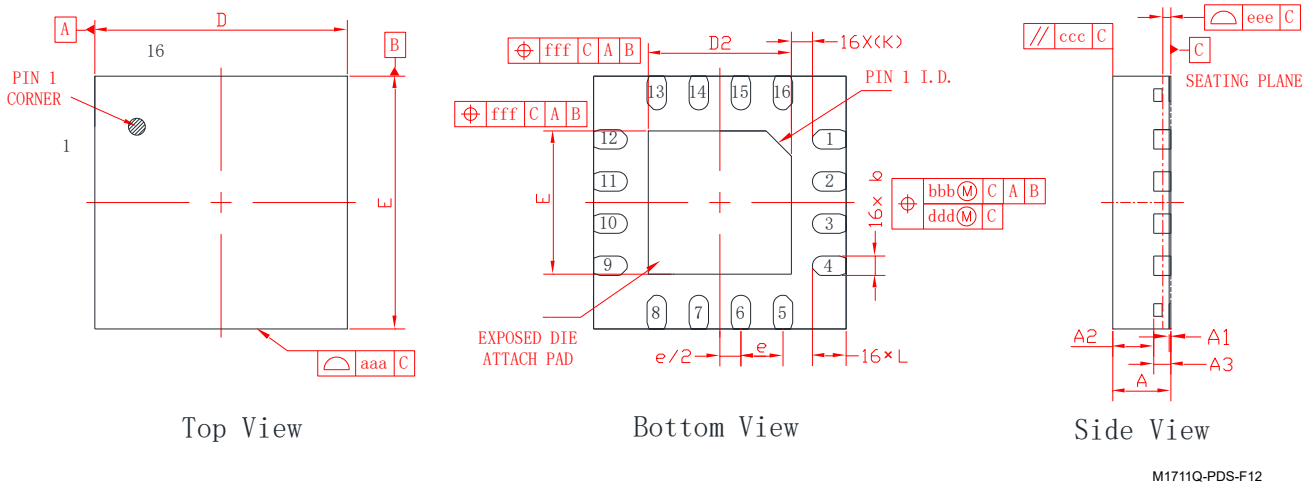


Figure 11. Output TOI vs. Frequency

9. Package Diagram



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.18	0.23	0.28
BODY SIZE	X	D		3 BSC	
	Y	E		3 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	D2	1.6	1.7	1.8
	Y	E2	1.6	1.7	1.8
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.25 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.1	
		bbb		0.05	
EXPOSED PAD OFFSET		fff		0.1	

- Dimensions shown in micrometre

Figure 12. M1711Q Package Information

Table 5. Pad Description

Pad	Symbol	Description
1, 2, 4, 8, 9, 11, 12, 16	NC	No internal connection. Recommend to GND at the PCB level
3	RF_{IN}	RF Input. 50Ohm. DC blocking capacitor is not required.
10	RF_{OUT}	RF Output. 50Ohm. DC blocking capacitor is not required.
5	V_{G1}	Gate Voltage;bias network is required (VG can be together at PCB)
6	V_{G2}	Gate Voltage;bias network is required (VG can be together at PCB)
7	V_{G3}	Gate Voltage;bias network is required (VG can be together at PCB)
13	V_{D3}	Drain Voltage;bias network is required (VG can be together at PCB)
14	V_{D2}	Drain Voltage;bias network is required (VG can be together at PCB)
15	V_{D1}	Drain Voltage;bias network is required (VG can be together at PCB)

10. Application Circuit

■ Application Circuit

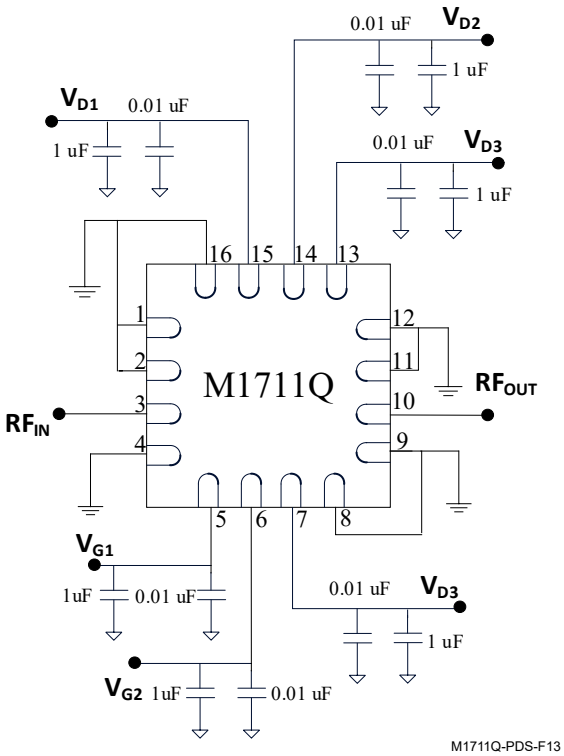


Figure 13. M1711Q Application Circuit

Table 6. Bias Procedure

Bias-up Procedure	Bias-down Procedure
1) Set V_G (externally connected V_{G1},V_{G2},V_{G3} together) to the pinch-off voltage, typically I_{DS}	1) Turn off RF signal
2) Turn on V_D (externally connected V_{D1},V_{D2},V_{D3} together) to nominal supply voltage (5V)	2) Turn off V_G
3) Slowly adjust V_G until I_{DS} current is attained	3) Wait two seconds to allow drain capacitor to discharge
4) Apply RF input power to desired level	4) Turn off V_D

11. Recommended Solder Temperature Profile

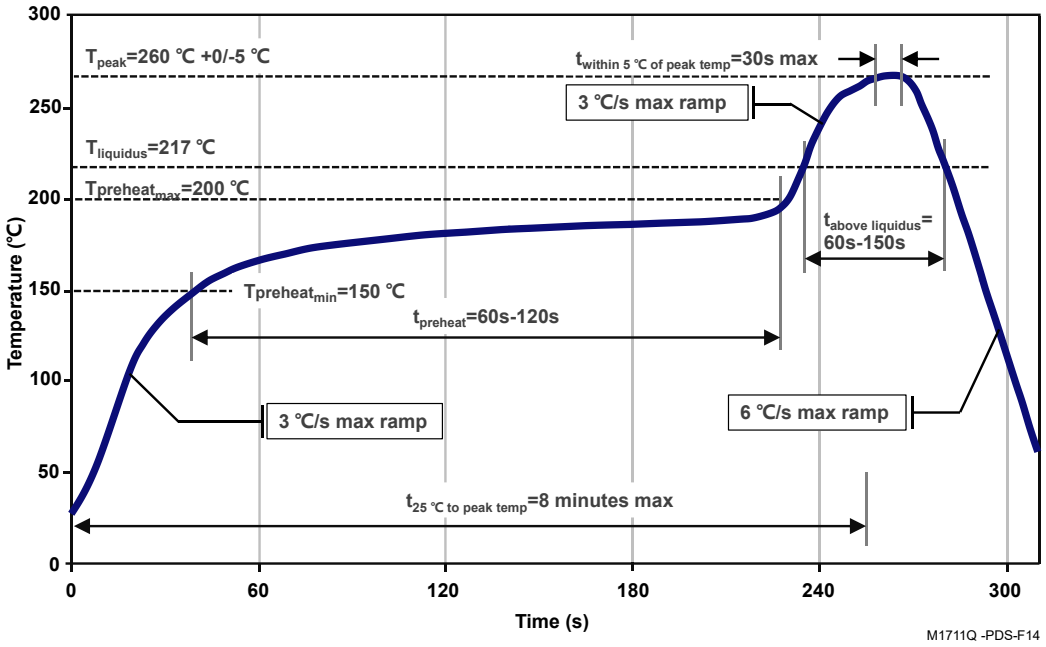


Figure 14. Recommended Solder Temperature Profile

12. Handling Precautions

- **ESD Caution**

  ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore proper ESD precautions should be taken to avoid performance degradation or loss of functionality.



13. Contact Information

For the latest specifications, additional product information, technical support and sales support, please contact:

- **Email:** RF.support@raytrontek.com
- **Web:** www.raytrontek.com

14. Disclaimer

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